Electronic Design Automation Tools (EDA) - Market Share Analysis, Industry Trends & Statistics, Growth Forecasts (2026 - 2031)

Market Report | 2026-01-16 | 120 pages | Mordor Intelligence

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Report description:

Electronic Design Automation Tools (EDA) Market Analysis

Electronic Design Automation Tools market size in 2026 is estimated at USD 20.78 billion, growing from 2025 value of USD 19.22 billion with 2031 projections showing USD 30.67 billion, growing at 8.1% CAGR over 2026-2031. The outlook builds on faster transistor scaling, AI-enabled design flows, and closer foundry-tool collaboration. Chip architects are shifting from manual rule tuning to data-driven optimization that shortens tape-out cycles and lowers re-spin risk. Cloud-based capacity bursting is widening access to advanced verification, while automotive functional-safety mandates push formal methods into mainstream design. The 2025 completion of Synopsys' USD 35 billion acquisition of Ansys signals a systemic move toward unified device-to-system platforms able to co-optimize silicon, package, and full-system performance simultaneously. Meanwhile, geopolitical export controls spur parallel EDA ecosystems, compelling vendors to certify flows for multiple regional foundries to avoid revenue erosion.

Global Electronic Design Automation Tools (EDA) Market Trends and Insights

Soaring Chip-Density in Advanced Nodes

Gate-All-Around transistors, backside power delivery, and multi-die packaging produce a ten-fold rise in design-rule checks compared with 7 nm processes. Foundries now co-develop flows with EDA leaders; Synopsys and TSMC certified full digital and analog toolchains for A16 and N2P nodes in April 2025. Unified exploration-to-signoff environments reduce costly re-spins-each

exceeding USD 50 million at 3 nm. Intel's 18A program likewise relies on integrated flows for 2.5D/3D architectures that merge compute, memory, and I/O on a single substrate.

Proliferation of AI/ML Accelerators and Custom SoCs

Hyperscale and edge providers increasingly commission purpose-built inference silicon. Cadence posted 40% YoY growth in semiconductor IP revenue in Q1 2025, attributing momentum to AI and chiplet projects. NVIDIA, ASML, TSMC, and Synopsys reported 40? lithography simulation speed-ups through the CuLitho software stack, enabling reticle layouts that meet AI power-per-watt targets. As accelerator heterogeneity rises, SIP reuse and on-package interconnect standards intensify demand for IP verification.

Escalating Licensing Costs for Leading EDA Suites

Annual enterprise bundles for comprehensive 3 nm sign-off now exceed USD 1 million per seat, forcing mid-tier fabs to prioritize tool modules and extend refresh cycles. Oligopolistic supply means price leverage remains with vendors, particularly for timing closure and lithography simulation packages that have no open-source substitute.

Other drivers and restraints analyzed in the detailed report include:

Rise of Cloud-Native EDA Workflows (EDA-as-a-Service)Automotive ISO 26262 Functional-Safety Compliance NeedsTalent Shortage in Sub-5 nm Physical-Design Engineers

For complete list of drivers and restraints, kindly check the Table Of Contents.

Segment Analysis

Semiconductor Intellectual Property (SIP) posted a 9.7% CAGR forecast, the fastest among tool categories, owing to rising chiplet architectures that favor verified interface blocks and mixed-signal cores. In 2025, SIP accounted for 18.74% of the Electronic Design Automation Tools market revenue, yet its attach rate per project has doubled since 2023 as foundries promote known-good-die strategies. The Electronic Design Automation Tools market size for SIP applications is projected to grow at a significant rate by 2031, underscoring the shift from monolithic SoCs to heterogeneous assembly.

IC Physical Design and Verification retained a 35.82% share thanks to the mandatory nature of placement, routing, static-timing, and DRC in every tape-out. However, AI-enhanced floorplanning automates multi-objective optimization, shrinking turnaround time by 30% on recent 3 nm designs.

Front-End Design tools record a 9.35% CAGR as high-level synthesis (HLS) and natural-language-to-RTL generators improve productivity. The Electronic Design Automation Tools market size for RTL automation is projected to grow significantly by 2031 on the back of AI-assisted code generation that captures functional intent in fewer iterations. Layout, Routing, and Timing Closure still governs 32.10% of the Electronic Design Automation Tools market share, reflecting the irreplaceable nature of sign-off-caliber timing convergence and advanced 3D parasitic extraction.

Generative design platforms now produce placement guidance that reduces wire length by 11% and leakage by 9% versus human scripts. Yet final SOC hand-off still relies on certified timing and electrical-rule reports accepted by foundries, cementing the relevance of established back-end toolchains.

The Electronic Design Automation Tools Report is Segmented by Tool Type (Computer-Aided Engineering, IC Physical Design and

Verification, and More), Design-Flow Stage (Front-End Design RTL, and More), Deployment Mode (On-Premise, and Cloud-Based), End-User Industry (Communication Infrastructure, Consumer Electronics, and More), and Geography (North America, and More). The Market Forecasts are Provided in Terms of Value (USD).

Geography Analysis

Asia-Pacific held a 42.05% share in 2025 and advances at a 9.55% CAGR to 2031. Foundry clustering in Taiwan and South Korea anchors regional tool demand, while China accelerates sovereign EDA stacks in response to U.S. export controls. State-backed initiatives channel subsidies toward AI-assisted place-and-route engines and SPICE simulators, aiming to localize flows before 3 nm production ramps. India leverages a large engineering base; design-service firms there grew 17% in 2024 as Western customers sought cost-effective RTL and DFT support.

North America retains influence through leadership in AI algorithms, IP catalogs, and cloud infrastructure. The region's share contracted slightly to 29.15% in 2025, yet remains the primary source of reference tool flows for leading-edge nodes. Export-control regimes require vendors to implement license-key geofencing, adding compliance cost but also locking in North American IP chains. Collaboration between Intel Foundry and Synopsys on 18A certified flows reinforces the U.S. bid to regain advanced manufacturing share. Europe focuses on automotive and industrial applications, with ISO 26262 driving premium verification tool adoption. TSMC's 2025 design center launch in Munich aims to embed foundry engineers within the regional supply chain, providing first-hand support for 3D-IC packaging and power-efficient AI accelerators. The EU Chips Act grants emphasize RandD tax credits for electronic-design clusters, further stimulating regional EDA uptake. Middle East and Africa and South America remain nascent, but showing double-digit growth where government fab projects or IoT rollouts emerge.

List of Companies Covered in this Report:

Ansys Inc. Cadence Design Systems Inc. Synopsys Inc. Siemens Digital Industries Software (Mentor Graphics) Keysight Technologies Inc. Altium Limited Zuken Ltd. Xilinx Inc. (AMD Adaptive and Embedded Computing Group) Aldec Inc. Agnisys Inc. Lauterbach GmbH Silvaco Inc. Real Intent Inc. Axiomise Ltd. Imperas Software Ltd. PDF Solutions Inc. Flex Logix Technologies Inc. Andes Technology Corp. Cobham Gaisler AB Arteris Inc.

Additional Benefits:

The market estimate (ME) sheet in Excel format
3 months of analyst support

Table of Contents:

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